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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,903	02/28/2002	Andy Wei	AMDI:115\HON	4163

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EXAMINER
LEE, HSIEN MING

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,903	WEI ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☒ Claim(s) *28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Remarks

1. Claims 1-33 are pending in the application.

2. No amendments have been submitted prior to this Office action.

3. The indication of allowable subject matters is withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-18, and 20-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshimi et al. (US 5,698,869).

In re claims 1, 4, 7 and 11, Yoshimi et al., in Fig. 7 and related text in col. 4, lines 15-33, expressly teach the claimed method of processing, comprising:

- forming an impurity region 206 (n+ region) in a device region of a semiconductor-on-insulator substrate (i.e. SOI.MOSFET device), the impurity region 206 defining a pn junction 215 and
- forming at least two dislocation regions D in the device region, the dislocation regions D traversing the pn junctions 215 (col. 4, lines 30-33); and
- forming a gate electrode 205 on the device region.

In re claims 2-3, 8-9, Yoshimi et al also teach that the forming of the impurity region comprises forming a source/drain extension region 206 and another impurity region 207

overlapping the source/drain extension region 206, wherein the source/drain extension region 206 and the another impurity region 207 are formed by ion implantation, i.e. germanium ions are implanted.

In re claims 5 and 12, Yoshimi et al also teach that the forming of the dislocation regions D comprises forming an amorphous region in the device region and heating the semiconductor-on-insulator substrate to recrystallize the amorphous region (col. 34, lines 58-61 and col. 35, lines 1-16).

In re claims 6 and 13, Yoshimi et al further teach that the forming of the amorphous region comprises implanting a neutral species ions (i.e. germanium ions) into the device region (col. 4, lines 15-22).

In re claim 10, Yoshimi et al. also teach that a first of the at least two dislocation regions D (i.e. the dislocation at the left side of a region 203) traverses a portion of the junction 215 proximate the source/drain extension region 206 and a second of the at least two dislocations D (i.e. the dislocation at the right side of a region 203) traverses a portion of the junction 215 proximate the another impurity region 206.

In re claims 14, 17, Yoshimi et al., in Fig. 7 and related text in col. 4, lines 15-33, teach the claimed method of processing, comprising:

- forming a first impurity region (i.e. 206 at the left side of 203) and a second impurity region (i.e. another 206 at the right side of 203) in a device region of a semiconductor-on-insulator substrate, the first impurity region defining a first junction 215 and the second impurity region defining a second junction 215;

- forming a first dislocation region D in the device region, the first dislocation region D (i.e. the D at left side of 203) traversing the first junction 215; and
- forming a second dislocation region D in the device region, the second dislocation region D (i.e. the D at right side of 203) traversing the second junction 215.

In re claims 15-16, Yoshimi et al also teach that the forming of the first impurity region comprises forming a first source/drain extension region 206 (i.e. the 206 at left side of 203) and a first overlapping impurity region 207 overlapping the source/drain extension region 206, and the forming of the second impurity region comprises forming a second source/drain extension region 206 (i.e. the 206 at right side of 203) and second overlapping impurity region 207 overlapping the second source/drain extension region 206, wherein the first and second source/drain extension region 206 and the first and second overlapping impurity region 207 are formed by ion implantation, i.e. germanium ions are implanted.

In re claim 18, Yoshimi et al also teach that the forming of the first and second dislocation regions D comprises forming a first amorphous region and a second amorphous region in the device region and heating the semiconductor-on-insulator substrate to recrystallize the first and second amorphous regions (col. 34, lines 58-61 and col. 35, lines 1-16).

In re claim 20, Yoshimi et al further teach that the forming of the first and second amorphous regions comprises implanting a neutral species ions (i.e. germanium ions) into the device region (col. 4, lines 15-22).

In re claims 21-27, with the aforementioned teachings, Yoshimi et al. disclose a circuit device, wherein the circuit device comprises a gate electrode 205, comprising:

- a semiconductor-on-insulator substrate having a device region;

- an impurity region 206/207 in the device region, the impurity region 206/207 defining a junction 215, wherein the impurity region 206/207 comprises an extension region206 and an overlapping region207; and
- a dislocation region D in the device region, the dislocation region D traversing the junction 215 proximate the extension region 206 and the overlapping region 207, wherein the circuit device comprises a plurality of dislocation regions D traversing the junction 215 and the device region comprises silicon.

In re claims 28-33, with the aforementioned teachings, Yoshimi et al. further disclose a circuit device, wherein the circuit device comprises a gate electrode 205, comprising:

- a semiconductor-on-insulator substrate having a device region;
- a first impurity region 206/206 in the device region (i.e. the region 206/207 at the left side of 203), the first impurity region 206/207 having a first extension region 206 and defining a first junction 215 (i.e. the first 215 at the left side of 203);
- a second impurity region 206/206 in the device region (i.e. the region 206/207 at the right side of 203), the second impurity region 206/207 having a second extension region 206 and defining a second junction 215 (i.e. the second 215 at the right side of 203), the second junction 215 being separated from the first junction 215 to define a channel 203;
- a first dislocation region D in the device region (i.e. the D at the left side of 203), the first dislocation region D traversing the first junction 215 proximate the first extension region 206 and the first overlapping region 207; and

- a second dislocation region D in the device region (i.e. the D at the right side of 203), the second dislocation region D traversing the second junction 215 proximate the second extension region 206 and the second overlapping region 207, the circuit device comprises a first plurality of dislocation regions D (i.e. the plurality of dislocation regions D at left side of 203) traversing the first junction 215 and a second plurality of dislocation regions D (i.e. the plurality of dislocation regions D at right side of 203) traversing the second junctions 215; and the device region comprises silicon.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimi et al. (US '869), specifically the prior art taught in Fig. 7 and related text , in view of remaining embodiments of Yoshimi et al. (US '869).

Yoshimi et al. in Fig. 7 is silent as to whether the first dislocation region D (i.e. the dislocations at left side of 203) is formed before the second dislocation region D (i.e. the dislocations at right side of 203).

However, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to optimize the process so that the first dislocation region D is formed before the second dislocation region D, since the optimization can be achieved by manipulating

ion implantation dose due to the fact that the dislocations are formed by lattice misfits via implanting germanium ions into the device region (col. 4, lines 15-25).

Claim Objections

8. Claim 28 is objected to because of the following informalities: editorial error.

At line 16 of page 15, "the first impurity" should be -- the first impurity region --.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 703-305-7341. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Hsien-Ming Lee
Examiner
Art Unit 2823

Sep. 9, 2003.